REMARKS

Claims 28 to 31 have been amended. Claims 27 to 32 remain active in this application.

Claims 28 to 30 were objected to. These claims have been amended as kindly suggested by the examiner to overcome the objection thereto.

Claims 27 to 32 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The amendments to claim 31 overcome this rejection and correct a grammatical error

Claims 27, 28 and 30 to 32 were rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (U.S. 6,709,901). The rejection is respectfully traversed both as previously presented and as amended to overcome the rejections under section 112.

Claim 31 requires, among other features, providing an added conductive region on the metallization pattern covering and conformal to each of the contact pads, the sidewalls of the windows and a portion of the protective overcoat surrounding the windows, the added conductive region having a planar outer surface, the outer surface of the added conductive region suitable to form metallurgical bonds without melting. No such feature is taught or suggested by Yamazaki et al. either alone or in the combination as claimed.

With reference to Fig. 10(B) of Yamazaki et al., the figure referred to in the rejection, it is clear that the structure does not meet the requirements of the method as claimed. The region 230 does not meet the requirements of claim 31 as set forth in the above paragraph since it is clearly not conformal to each of the contact pads, the

sidewalls of the windows and a portion of the protective overcoat surrounding the windows, the added conductive region having a planar outer surface, the outer surface of the added conductive region suitable to form metallurgical bonds without melting.

The above described feature is discussed at page 4, lines 10ff where it is stated "[e]ach of these contact pads has an added conductive layer on the circuit metallization. This added layer has a conformal surface adjacent the chip and a planar outer surface, and this outer surface is suitable to form metallurgical bonds without melting (underline not in original)". No such step or its benefits is taught or even remotely suggested by Yamazaki et al.

Claim 31 further requires providing an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of the contact pads, aligning the added metallization and the board pads so that each of the contact pads is connected to a corresponding board terminal pad and *metallurgically* bonding the chip metallization and the board pads without melting the outer surface of the added conductive layer. No such features are taught or suggested by Yamazaki et al. either alone or in the combination as claimed.

By the above claimed procedure, the board terminal pad is connected directly to the bond pad, thereby eliminating the required conductive particle 227 or barrier layer 229 of Yamazaki et al.

Claims 27, 28, 30 and 32 depend from claim 31 and therefore define patentably over Yamazaki et al. for at least the reasons stated above with reference to claim 31.

In addition, claim 27 further limits claim 31 by requiring that the step of depositing be selected from a group consisting of sputtering, evaporating, and plating. No such combination is taught or suggested by Yamazaki et al.

Claim 28 further limits claim 31 by requiring that the step of fabricating a planar outer surface of the added conductive layer comprise the step of depositing at least one added conductive layer by electroless plating. No such combination is taught or suggested by Yamazaki et al.

Claim 30 further limits claim 31 by requiring that the step of fabricating a planar outer surface of the added conductive layer comprise the step of depositing at least one added conductive layer by using the method of support by islands of protective overcoat. No such combination is taught or suggested by Yamazaki et al.

Claim 32 further limits claim 31 by requiring that the bonding comprise one of direct welding by metallic interdiffusion, attaching including solder paste and attaching including a conductive adhesive. No such combination is taught or suggested by Yamazaki et al.

Claim 29 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazakiet al. in view of Akram et al. (U.S. 6,617,687). The rejection is respectfully traversed.

Claim 29 depends from claim 31 and therefore defines patentably over the applied references for at least the reasons presented above with reference to claim 31 since Akram et al. fails to overcome the deficiencies of Yamazaki et al. as discussed above.

Claim 29 further limits claim 31 by requiring that the step of fabricating a planar outer surface of the added conductive region comprise the step of depositing a second of

at least one added conductive layer by screen printing. No such combination is taught or suggested by Yamazaki et al., Akram or any proper combination of these references.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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